	L #	Hit	S arch T xt	DB
1	L1	3381	(361/734,738,760,763,767,768,782,783,792,793,794,795).ccls.	USPAT; US-PGPUB
2	L2	4049	(257/686,691,700,723,724,777).ccls.	USPAT; US-PGPUB
3	L3	7026	1 2	USPAT; US-PGPUB
4	L4	586	3 and @pd>=20030205	USPAT; US-PGPUB
5	L5	160	4 and (capacitor$1 condenser$1)	USPAT; US-PGPUB
6	L6	6	5 and ((processor$1 microprocessor$1) same (communication$1 telecommunication$1))	USPAT; US-PGPUB
7	L7	154	5 not 6	USPAT; US-PGPUB

	L #	Hit	S arch T xt	DB
8	L8	126	7 and (die$1 dice chip$1)	USPAT; US-PGPUB
9	L9	8	("3795047" | "4916417" | "5164692" | "5359488" | "5525942" | "5851845" | "6177850" | "6258449" | "2002/0059723").PN.	USPAT
10	L10	28	7 not 8	USPAT; US-PGPUB

	L #	Hit	S arch T xt	DBs
1	L1	759	(361/306.1,306.2,306.3).ccls.	USPAT; US-PGPUB
2	L2	33	1 and (plated with (through$1hole$1 via$1))	USPAT; US-PGPUB
3	L3	311	361/321.2.ccls.	USPAT; US-PGPUB
4	L4	5	3 and (plated with (through$1hole$1 via$1))	USPAT; US-PGPUB
5	L5	1	1 and (lined with (through$1hole$1 via$1))	USPAT; US-PGPUB
6	L6	11	1 and ((electroplat$3 (electroless$2 adj plat$3)) with (through$1hole$1 via$1))	USPAT; US-PGPUB
7	L7	1064	428/210.ccls.	USPAT; US-PGPUB

	L #	Hit	S arch T xt	DB
8	L8	32	7 and (plat d with (through$1hole$1 via$1))	USP AT; US-P GPU B
9	L9	9	7 and ((electroplat$3 (electroless$2 adj plat$3)) with (through$1hole$1 via$1))	USP AT; US-P GPU B
10	L10	33	8 9	USP AT; US-P GPU B
11	L11	347	(conductive adj paste$1) and (plated with (through$1hole$1 via$1))	USP AT; US-P GPU B